

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 1, line 5 with the following:

This application is a Continuation of U.S. Application Serial No. 10/303,946 filed on November 26, 2002; which is a Continuation of 09/984,960 filed on October 31, 2001, hereby incorporated by reference as to its entirety. This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2000-333719, filed October 31, 2000, the entire contents of which are incorporated herein by reference.

Please replace the paragraph beginning on page 4 line 11 to page 8 line 4, with the following:

According to an aspect of the present invention, there is provided a semiconductor memory device comprising: a memory cell array including a plurality of memory cells arranged in rows and columns, the memory cell array having first word lines connected to a first group of memory cells in the plurality of memory cells, second word lines connected to a second group of memory cells in the plurality of memory cells which are adjacent to the first word lines, and third word lines connected to a third group of memory cells in the plurality of memory cells, and a word-line select circuit configured to select at least one row of memory cells from the plurality of memory cells, the word-line select circuit includes a first group, a second group and a third group of word-line select transistors arranged in row and column directions, the first group of word-line select transistors being each connected to an associated one of the first word lines, the second group of word-line select transistors being each connected to an associated one of the second word lines, the third group of word-line select transistors being each connected to an associated one of the third word lines, the third group of word-line select transistors are each interposed between any adjacent two of the first and second group of word-line select transistors.

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a memory cell array including a plurality of memory cells arranged in rows and columns, the memory cell array having first word lines connected to a first group of memory cells in the plurality of memory cells, second word lines connected to a second group of memory cells in the plurality of memory cells, and third word lines connected to a third group of memory cells in the plurality of memory cells, and a word-line select circuit configured to select at least one row of memory cells from the plurality of memory cells, the memory cell array having first word-line select transistors connected to the first word lines in the memory cell array to select the first word lines, respectively, second word-line select transistors connected to the second word lines to select the second word lines, respectively, and third word-line select transistors connected to the third word lines to select the third word lines, respectively, wherein the first word-line select transistors connected to the first word lines are separated from the third word-line select transistors connected to the third word lines in both the row and column directions, such that a first voltage is applied to the first word lines, a second voltage higher than the first voltage is applied to the second word lines, and a third voltage higher than the second voltage is applied to the third word lines.

According to still another aspect to the present invention, there is provided a semiconductor memory device comprising: a memory cell array including a plurality of memory cells arranged in rows and columns; and a word-line select circuit including word-line select transistors arranged in row and column directions, and configured to select at least one row of memory cells from the plurality of memory cells, the word-line select circuit including first transistors to which a first voltage is to be applied, second transistors to which a second voltage higher than the first voltage is to be applied, and third transistors to which a third voltage higher than the second voltage is to be

applied, the third transistors being separated from the first transistors.